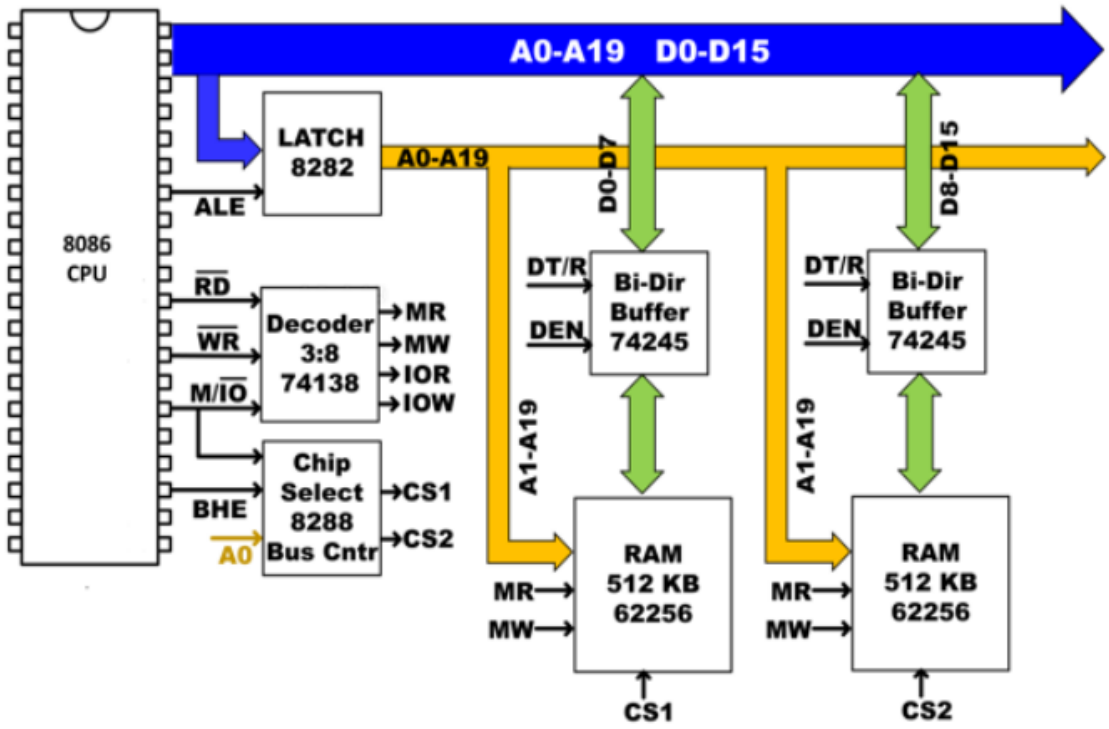
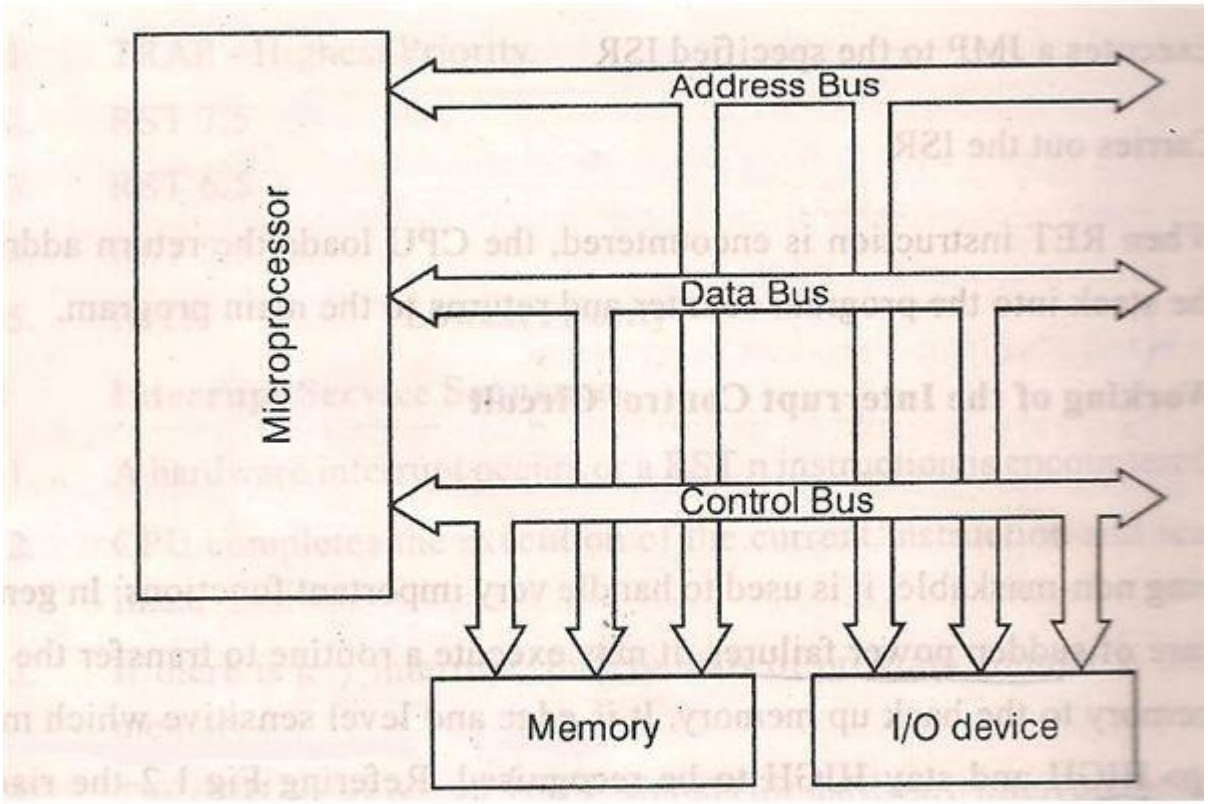
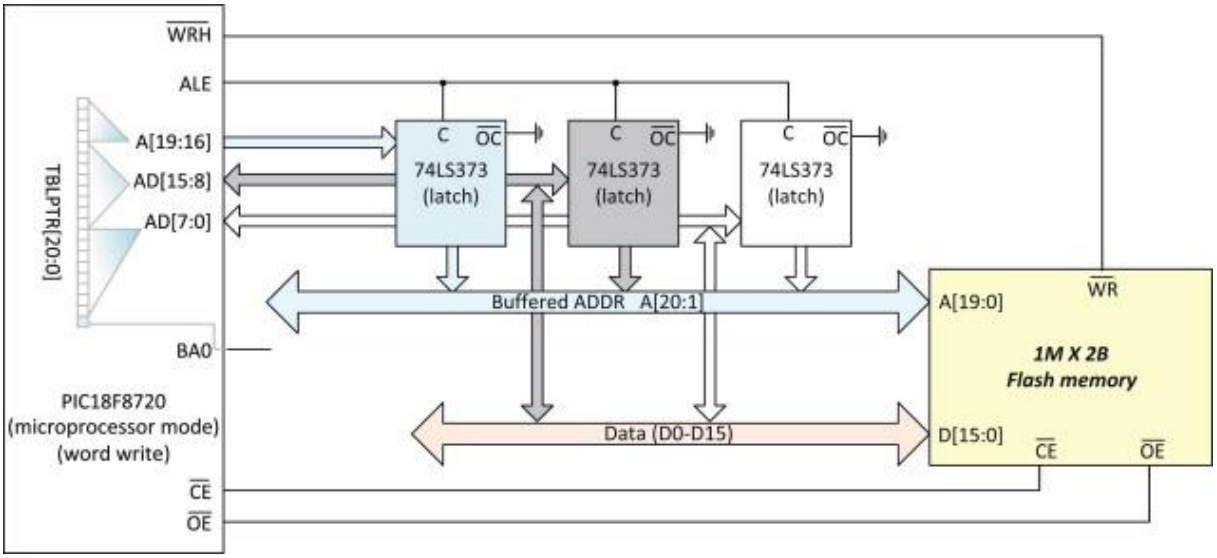
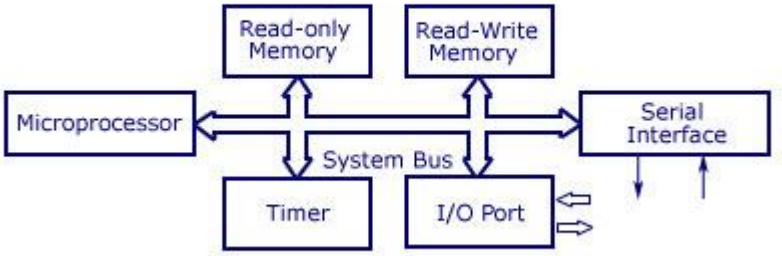
8086 Memory Organization



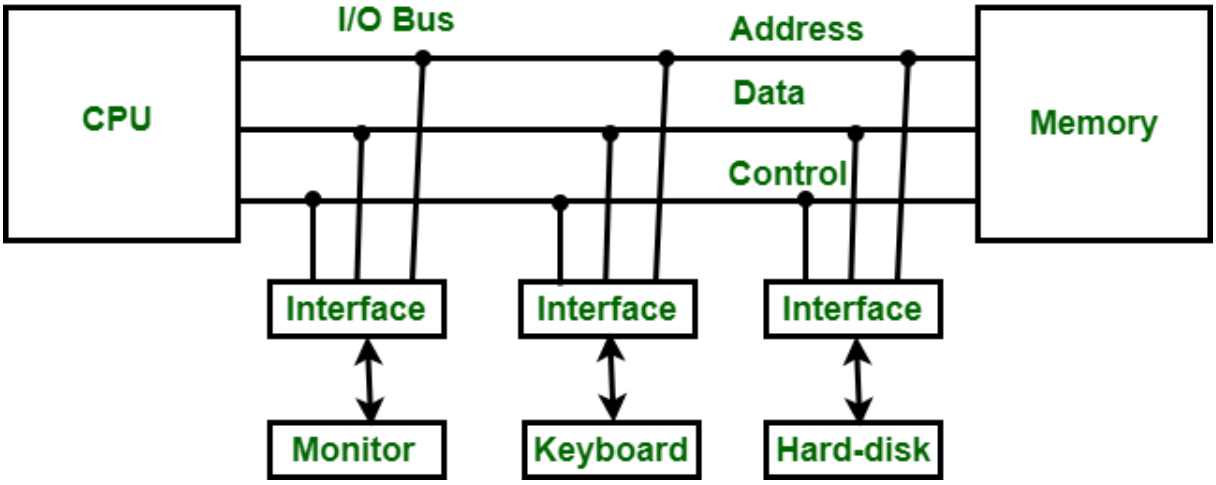

Address Bus
Microprocessor
Data Bus
Control Bus
Memory
I/O device


WRH
ALE
A[19:16]
AD[15:8]
AD[7:0]
TBLPTR[20:0]
BA0
PIC18F8720
(microprocessor mode)
(word write)
CE
OE
C
OC
74LS373
(latch)
74LS373
(latch)
74LS373
(latch)
Buffered ADDR A[20:1]
Data (D0-D15)
A[19:0]
WR
1M X 2B
Flash memory
D[15:0]
CE
OE

Schematic Arrangement of a Microprocessor Based System



www.CircuitsToday.com



CPU Connection to I/O Devices

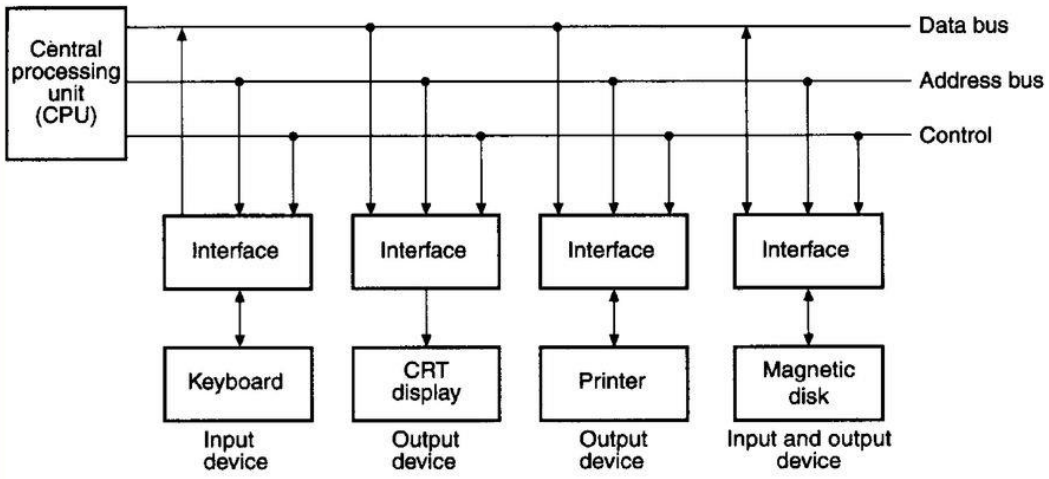
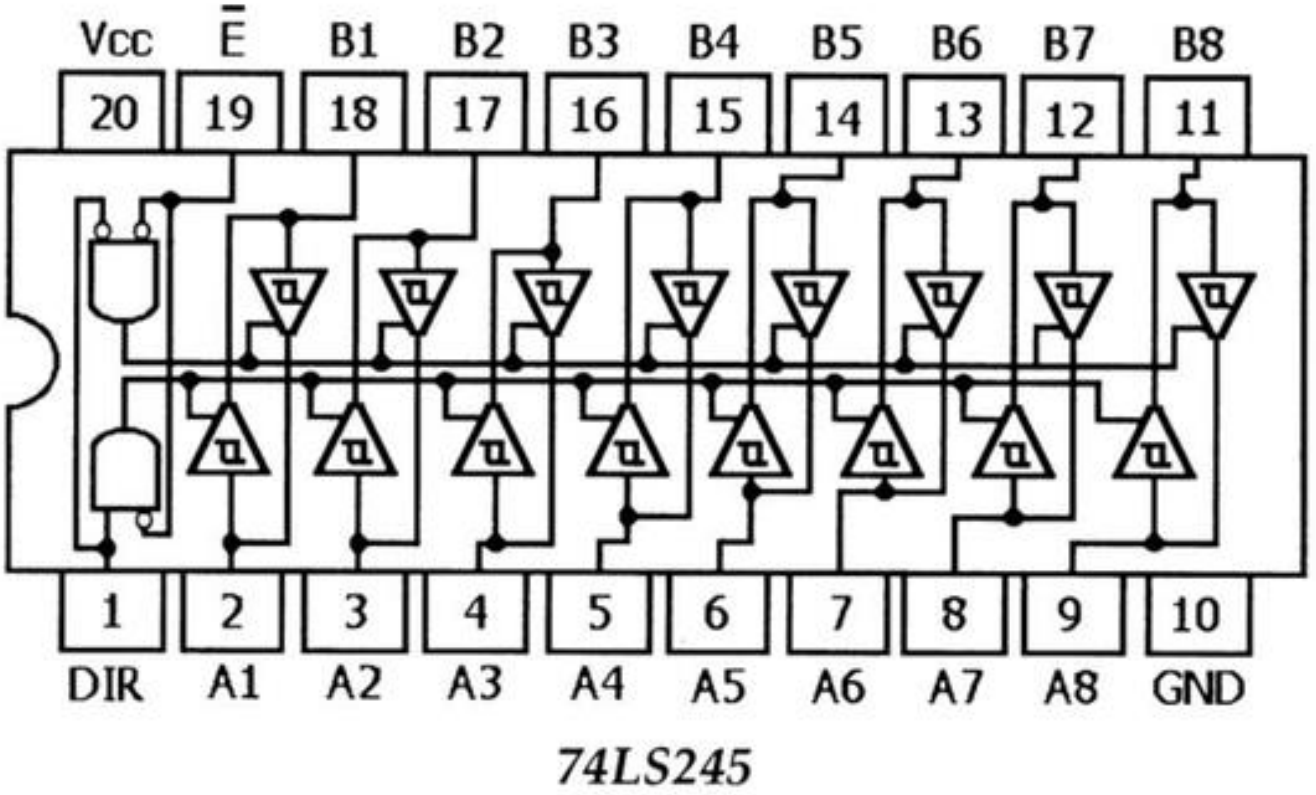


FIGURE 11-4
Connection of I/O Devices to CPU

Somme Interesting circuits Logiques for Microprocessor system Design

74Ls245

Brochage



Ref : https://www.datasheetarchive.com/74LS245%20buffer-datasheet.html

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The SNx4LS245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can disable the device so that the buses are effectively isolated.

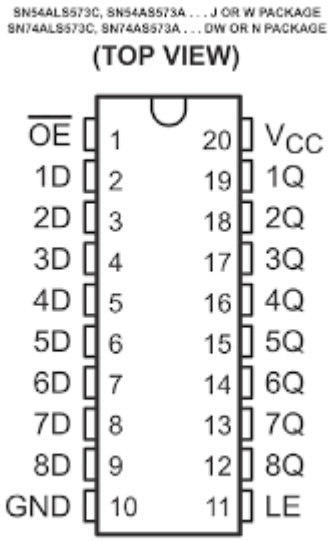
Applications

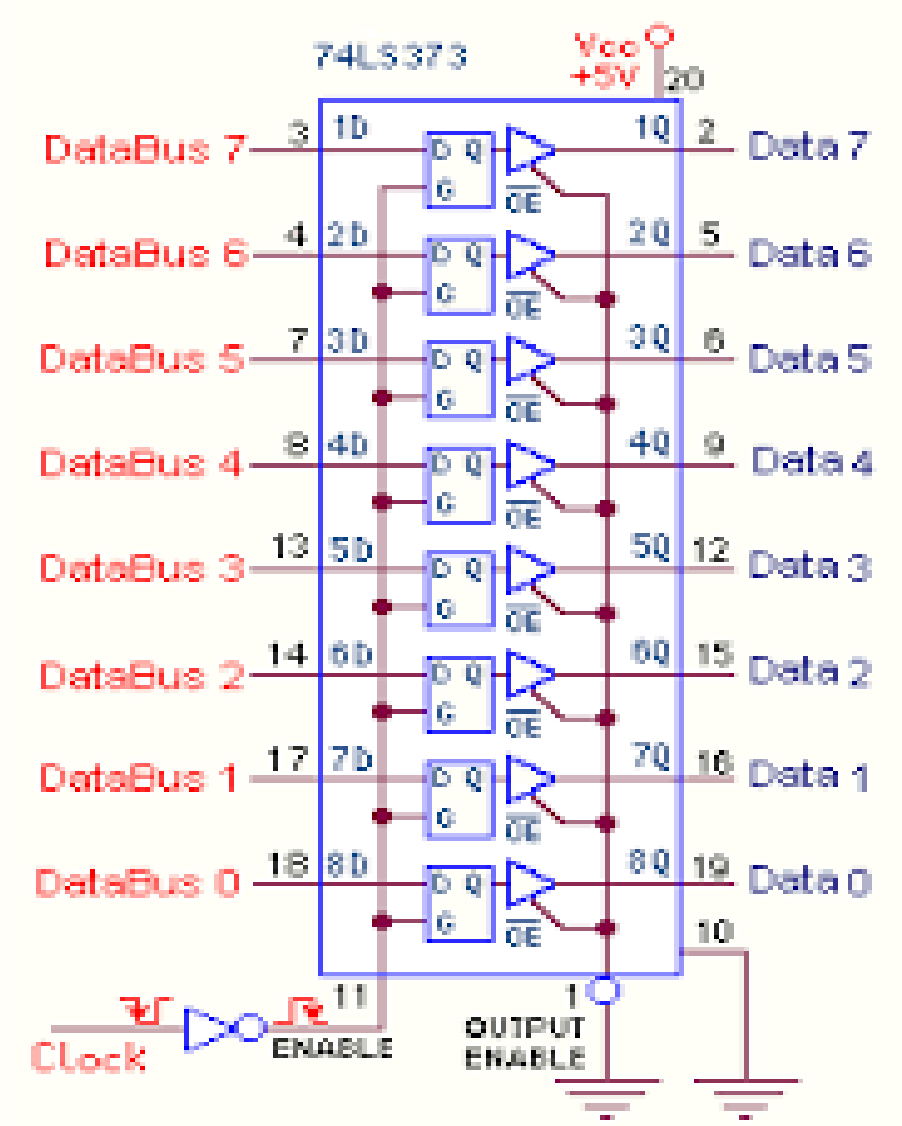
- Building Automation
- Electronic Point of Sale
- Factory Automation and Control
- Test and Measurement

Features

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- Hysteresis at Bus Inputs Improves Noise Margins
- Typical Propagation Delay Times Port to Port, 8 ns

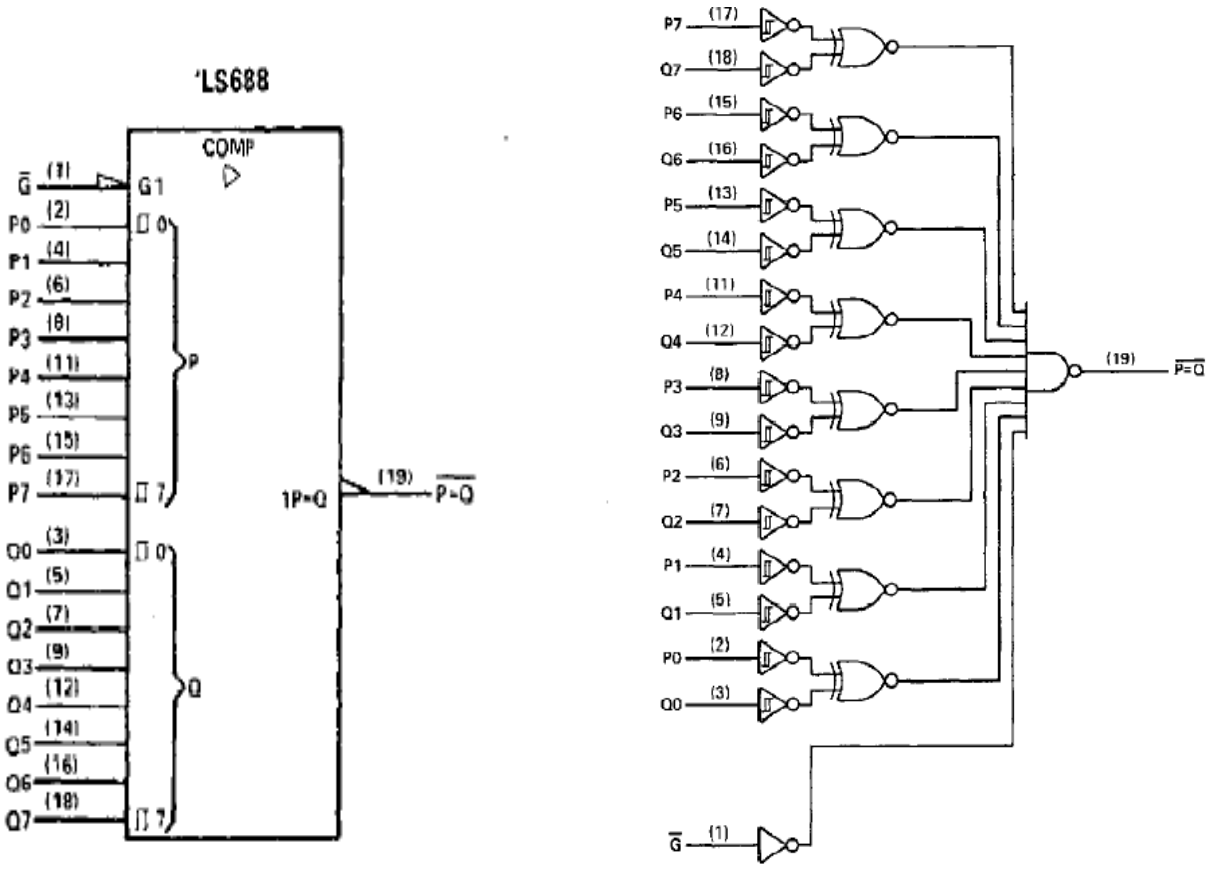
74LS 573 Latch



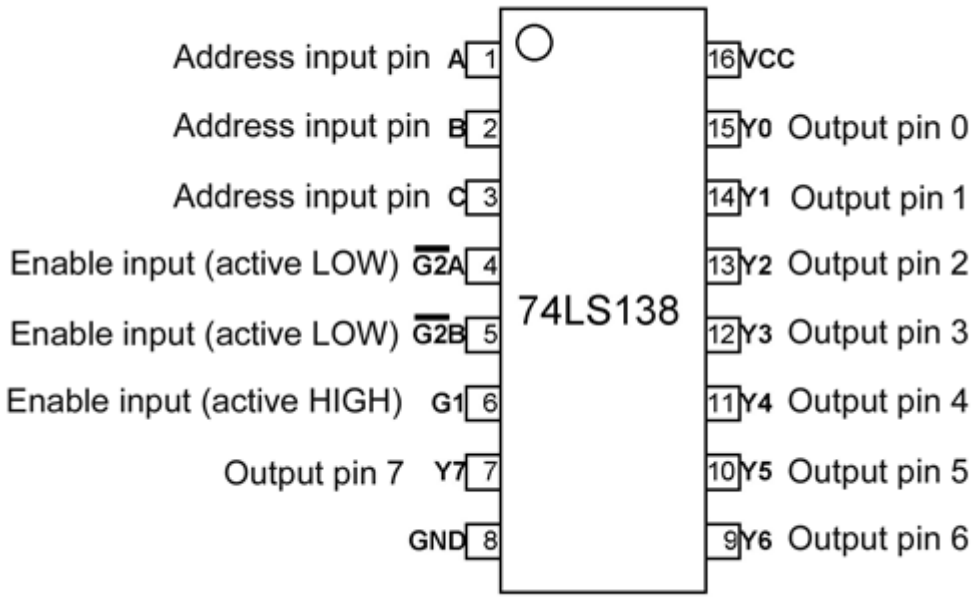


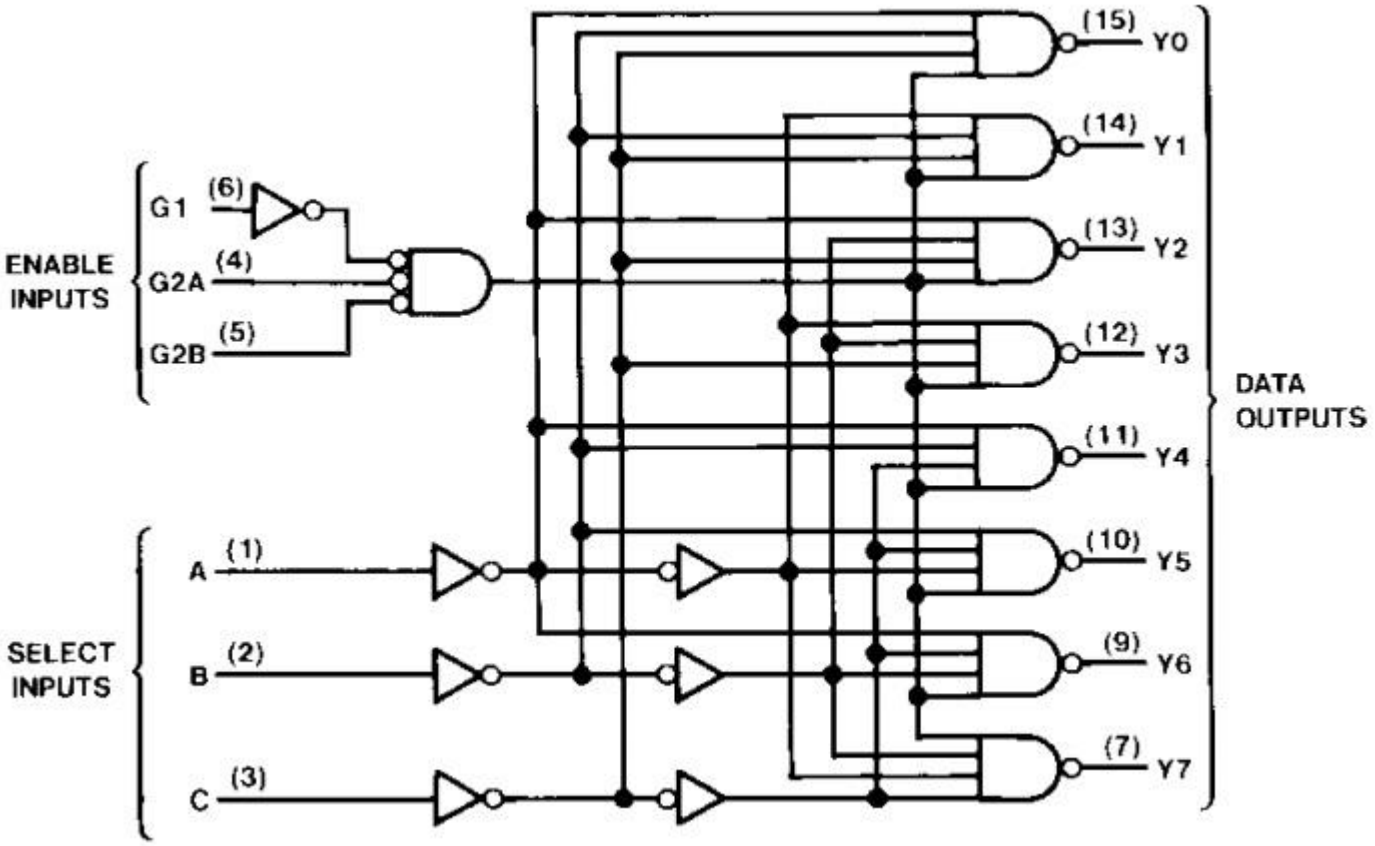
The ’LS573 is a high speed octal latch with buffered common Latch Enable (LE) and buffered common Output Enable (OE) inputs. This device is functionally identical to the ’LS373, but has different pinouts. For truth tables, discussion of operations and AC and DC specifications, please refer to the ’LS373 data sheet. Features n Inputs and outputs on opposite sides of package allowing easy interface with microprocessors n Useful as input or output port for microprocessors n Functionally identical to ’LS373 n Input clamp diodes limit high speed termination effects n Fully TTL and CMOS compatible

LS688 Comparateur



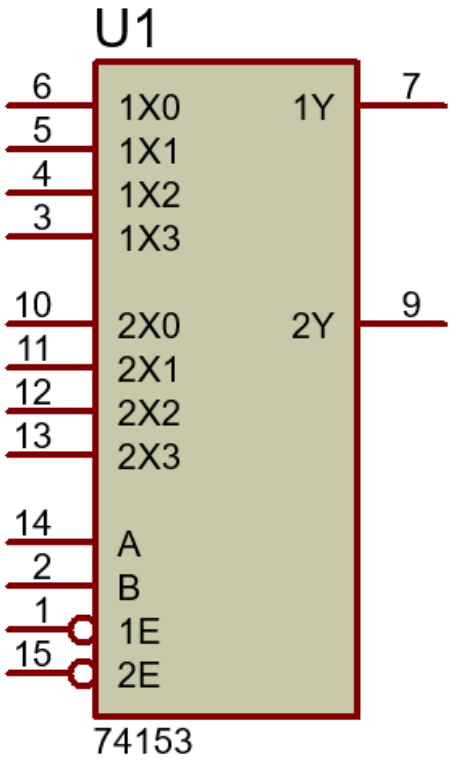
74LS138 3/8 Decoder

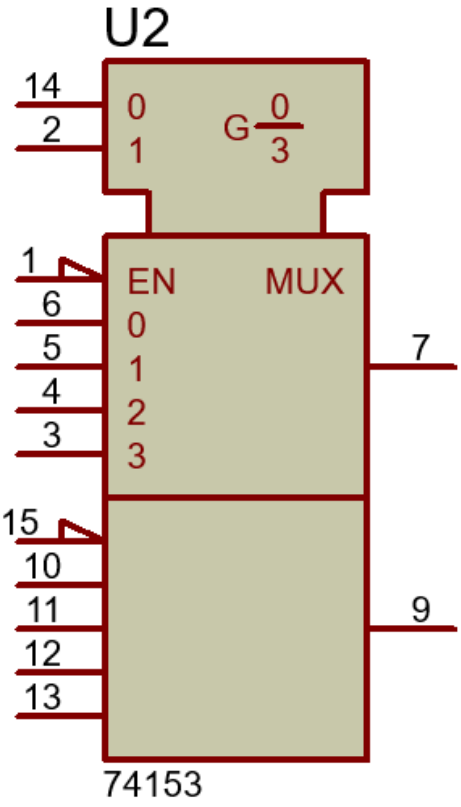


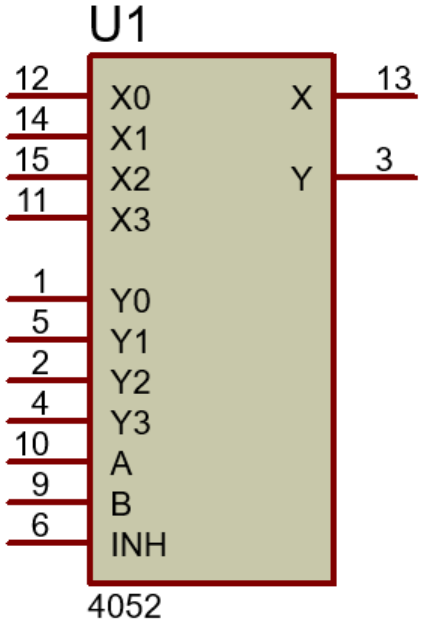


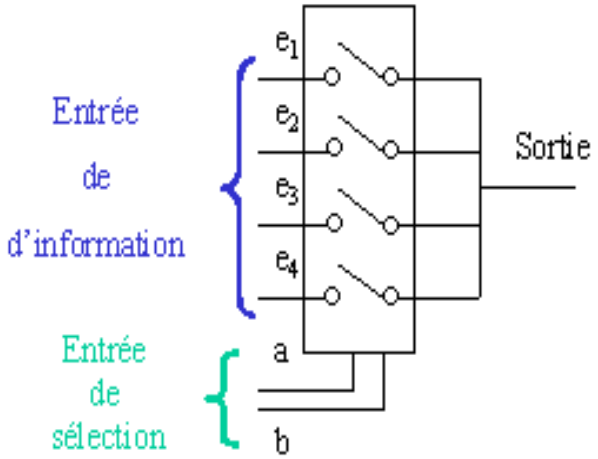
Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	YO	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

Mux- 74153


U1
6
5
4
3
10
11
12
13
14
2
1
15
1X0
1X1
1X2
1X3
2X0
2X1
2X2
2X3
A
B
1E
2E
1Y
2Y
7
9
74153


U2
14
2
1
0
1
G
0
3
1
6
5
4
3
15
10
11
12
13
EN
MUX
0
1
2
3
7
9
74153


U1
12
14
15
11
1
5
2
4
10
9
6
X0
X1
X2
X3
Y0
Y1
Y2
Y3
A
B
INH
X
Y
13
3
4052


Entrée
de
d'information
Entrée
de
sélection
e1
e2
e3
e4
a
b
Sortie