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TD2

✓ **Course reminder:**

Capacity=$2^{\text{number of address lines}} \times$ number of data lines
Transfer Rate=Frequency (in MHz)×Bus Width (in Bytes)

■ Exercice 1 :

We consider several types of memory characterized by:

A: the number of address lines / **D**: the number of data lines

1. Determine the total size of the memory in each of the following cases:

(a) D = 8 bits and A = 20
(b) D = 16 bits and A = 30
(c) D = 32 bits and A = 30

2. Express these sizes: in bits, then in bytes, and finally in words.
3. What happens to memory size if we double the number of address lines?
4. Determine the number of address bus lines and data bus lines for a memory of 16 MB with assumptions about its organization (byte-addressable or word-addressable)

■ Exercice 2 :

1/ A memory has 10 address lines and 8 data lines.

What is its capacity in bits?

2/ How many address lines are required to access 256 KBytes, knowing that each word is composed of one byte?

3/ Consider a main memory of 2 MB

Calculate the size of this memory when expressed in:

- 16-bit words
- 32-bit words

4/ Consider a computer with the following configuration:

- Main memory size: 1 MB
- Memory word size: 2 B
  → Calculate the address bus width (number of address lines) required to access this memory.

■ Exercice 3:

We have a Von Neumann system with a 24-bit address bus and a 2.4 GHz clock frequency.

1/ Draw the architecture and show the CPU, memory, and I/O devices connected by address, data, and control buses.

2/ Calculate the maximum memory capacity:
Find how much memory a 24-bit address bus can access (in Bytes, KB, MB, GB).

3/ Find the clock cycle time:
Compute the duration of one processor cycle at 2.4 GHz (in seconds).

4/ If a 32-bit CPU can access 4 GB of memory, what would be the required address bus width?

5/ Why does increasing the number of address lines exponentially increase memory capacity?