Ministry of Higher Education and Scientific Research
العلمي البحث و العالي التعليم وزارة

BADJI MOKHTAR-ANNABA UNIVERSITY
UNIVERSITE BADJI MOKHTAR-ANNABA

جامعة باجي مختار-عنابة

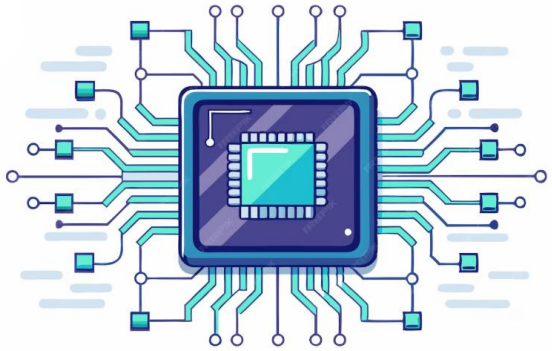
Faculty of technology
Electronics departement

Embedded Computing Systems course

Teaching method : Distance learning

Chapter 2
Microprocessor intel 8085

Course 4



Teaching by
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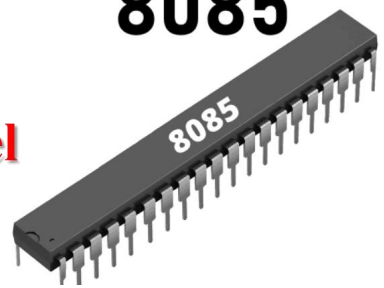
Promotion : 2025/2026

- To better understand the operation of microprocessor-based systems, we chose to study the Intel 8085, a classic and educational model.

Its simple architecture effectively illustrates the core principles of microprocessor design, instruction execution, and data interaction between the processor, memory, and peripherals.

8085



❖ Microprocessor Intel

Release Year	**1976**
Data Bus width	8-bit
Adress Bus width	16- bit (64KB memory addressing)
Instruction Set	3Mhz
Type	8-bit Microprocesssor
Registers	8-bit general-purpose registers

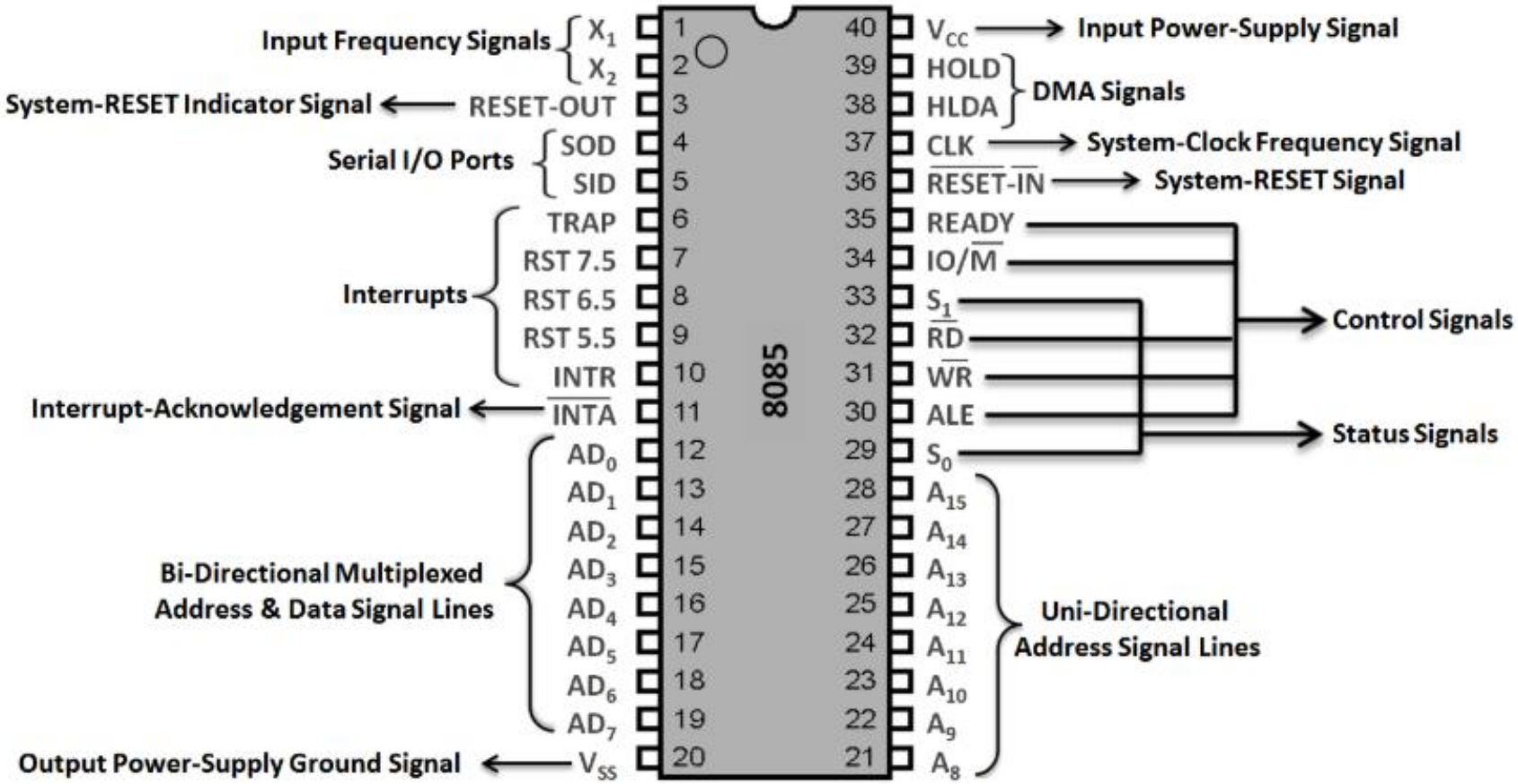


Fig.No.1:Pin-Diagram of 8085 Microprocessor

The signals of this 40 pin is grouped into 6 categories:

- Power supply and clock signals
- Data/ Address buses
- Serial I/O ports
- Control and status signals
- Interrupts and externally generated signals
- Direct memory access

- **PIN 1, 2:** X1, X2 → These pins are connected to an external crystal oscillator to operate the internal clock generator. The input frequency is divided by 2 to provide the working frequency for the processor;

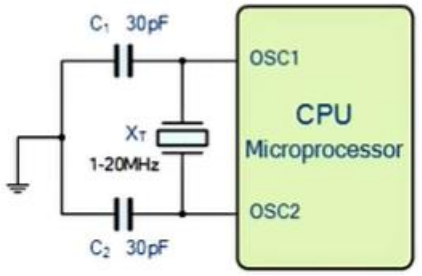
If the crystal connected between X1 and X2 has a frequency of 6 MHz,

→ the 8085 operates internally at 3 MHz.

- **PIN 3:** RESET OUT → This pin indicates that the CPU is being reset. It is an output pin and can be used as a working or indicating signal from the microcontroller to perform a task when the microprocessor is reset.
- **PIN 4:** SOD (Serial Output Data) → This is an output pin used for serial communication Used to send serial data to an external device;
- **PIN 5:** SID (Serial Input Data) → This is an input pin, also used for serial communication, used to receive serial data from an external device;
- **PIN 6:** TRAP → This is an input pin sensitive to a non-maskable restart interrupt (NMI), also called a trap interrupt. It is recognized by the microprocessor along with INTR or RST interrupts but has the highest priority among all interrupts.
- **PIN 7, 8, 9:** RST 5.5, RST 6.5, RST 7.5 → These are input pins used to cause an immediate restart of the microprocessor. These interrupts can be masked and have a higher priority than INTR.

Crystal Oscillator

A **crystal oscillator** is an electronic circuit that uses a quartz crystal to generate a **stable and precise frequency**.



- **PIN 10: INTR** → This is an input pin used to create a general-purpose interrupt request. It is recognized during the next-to-last clock cycle and also during HOLD and HALT states. This interrupt can be controlled by software, and when accepted, the INTA signal is issued. Among all interrupts, it has the lowest priority.
- **PIN 11:** INTA → This is an output pin activated when an INTR request is accepted. It can be used as a signal for other microcontrollers or ICs to perform tasks at that time.
- PIN 12–19: AD0–AD7 → These are multiplexed address/data bus pins, used for both input and output operations.
- PIN 20: VSS → Ground pin connected to the lower potential of the power supply.
- **PIN 21–28: A8–A15** → These are address bus output pins, holding the upper 8 bits of the memory address.
- PIN 29, 33, 34: S0, S1 & IO/$\overline{M}$ → These output pins indicate the status of the machine cycle. In combination (truth table), they represent the current status of the IC 5 instruction Cycle); These signals show the type of recent operation of the microprocessor. The table below represents the status of the data bus under different conditions:

IO/M'	S1	S0	Data Bus Status
0	1	1	Opcode fetch
0	1	0	Memory read
0	0	1	Memory write
1	1	0	I/O read
1	0	1	I/O write
1	1	1	Interrupt acknowledge
0	0	0	Halt

- PIN 30: ALE (Address Latch Enable) → This is an output pin activated during the first clock state of a machine cycle. It enables the address to be latched (stored) into the on-chip latch of peripherals.
- **PIN 31:** $\overline{WR}$ → This is a write control output pin (active low). It indicates that data is to be written onto the data bus or the selected memory location.
- **PIN 32:** $\overline{RD}$ → This is a read control output pin (active low). It indicates that the data bus is ready for data transfer, i.e., to read from the selected memory location or I/O device.
- **PIN 35: READY** → This is an input pin that is high during the read and write cycles to indicate that the bus and memory are ready to send or receive data. If this pin is low, the CPU will wait until it goes high before completing the read/write cycle.
- **PIN 36: RESET IN** → This input pin resets the CPU by setting the program counter to 0 and resetting the interrupt enable and HLDA flip-flops. It must be kept high for at least 3 clock cycles. The CPU remains in the reset state while this signal is applied.
- **PIN 37: CLK** → This is the system clock output pin. Its time period is twice that of the crystal oscillator input.
- **PIN 38:** HLDA (Hold Acknowledge) → This output pin indicates that the CPU has received a HOLD request and will release the buses in the next clock cycle.
- **PIN 39: HOLD** → This input pin signals the CPU that another master device is requesting the address and data buses. Upon receiving this request, the CPU clears both buses after completing the current data transfer.
- **PIN 40:** VCC → This is the power supply pin, which must be connected to +5V for the instruction cycle and overall CPU operation.

Address/ Data Buses

- **Address Bus:** This category contains 8 pins.

The address bus has 16 lines i.e.; it can carry 16 bits at a time. However, out of 16, 8 are multiplexed with the data bus and the leftover 8 are separately shown by pin number 21 to 28 in the pin configuration.

These are used to carry the address of data and instruction from the processor to the memory location and is unidirectional in nature. These are denoted by A8 to A15 that represents the 8 MSB of the memory location or input-output address.

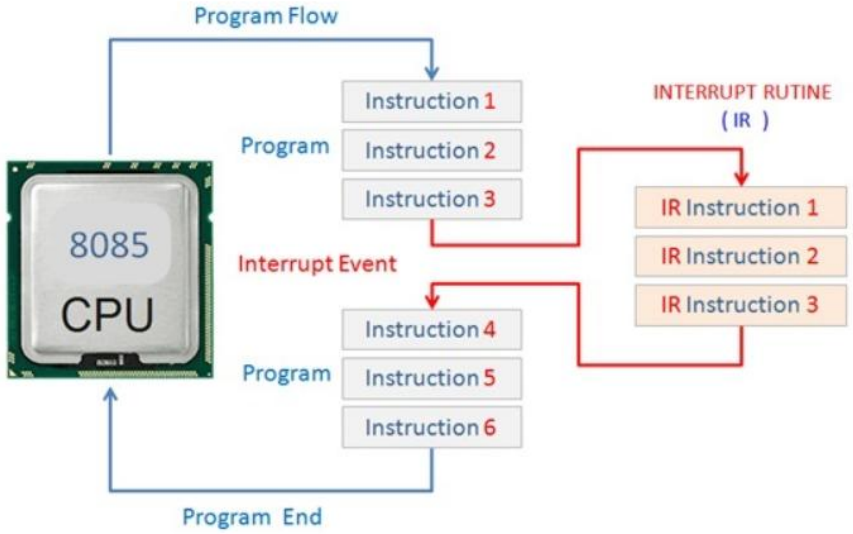
- **Data Bus with multiplexed address bus:** This category also contains 8 pins.

The size of the data bus of the 8085 microprocessor is 8 bits. However, to reduce the number of bus lines these 8-bit data bus lines are multiplexed with the 8-bit address bus.

These are shown by pin number 12 to 19. The address bus is denoted by A whereas the data bus is denoted by D. The pin configuration denotes the lower order multiplexed address and data bus bits from AD0 to AD7.

❖ Interrupts

Interrupts are the signals that are generated to break the sequence of an ongoing operation. When an interrupt signal is generated then CPU immediately stops its recent task under operation and switches to some other program known as interrupt service routine (ISR).



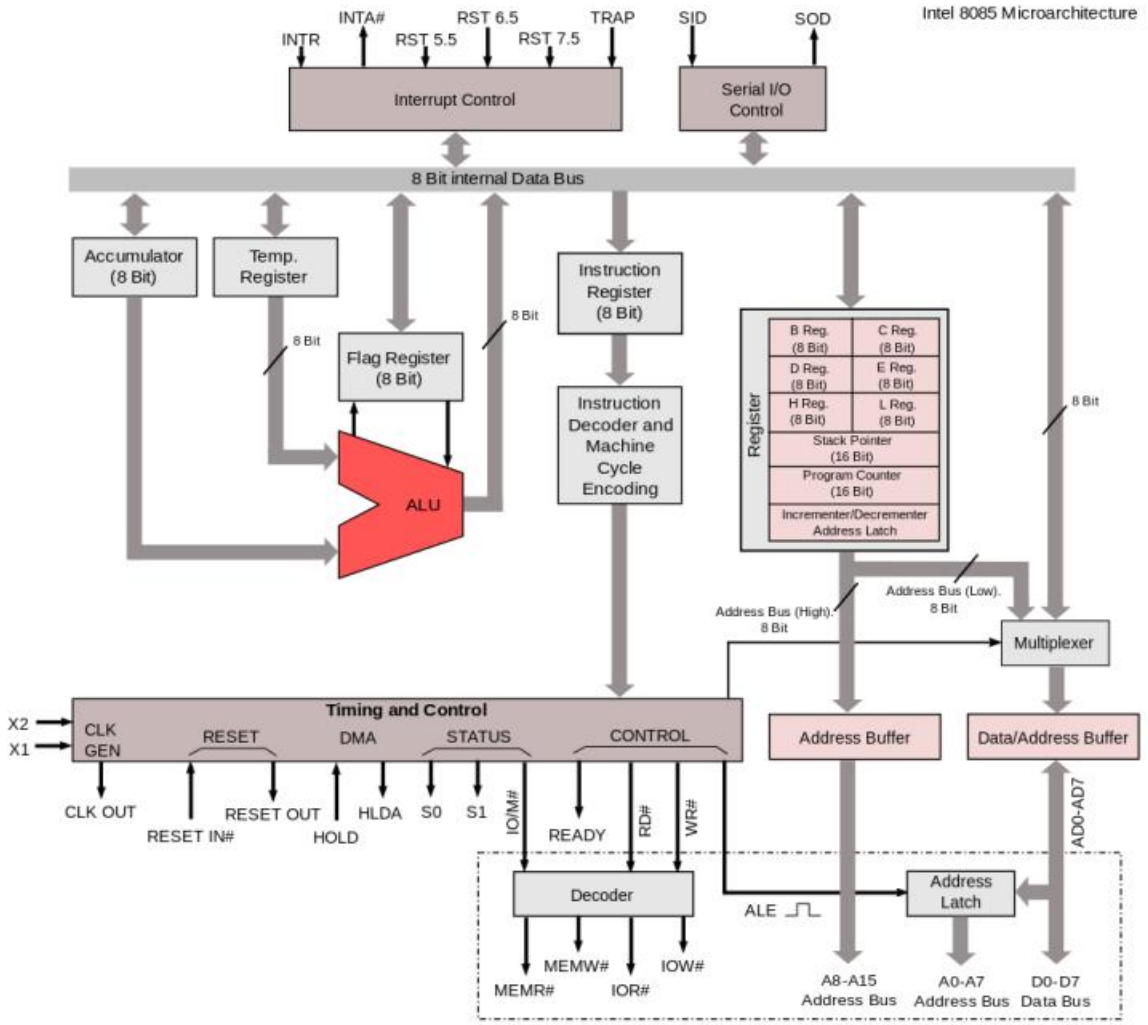
However, after the CPU gets back to its main program for execution.

In the pin configuration, 5 types of interrupts are shown ; there exist 2 types of interrupts: **Maskable Interrupt** and **Non-maskable interrupt**

Out of the 5 major interrupts 4 are the maskable interrupts. These are INTR, RST5.5, RST6.5, RST7.5 and are easily manageable interrupts.

However, TRAP is a non-maskable interrupt and holds the topmost priority among all interrupts in the 8085 microprocessor.

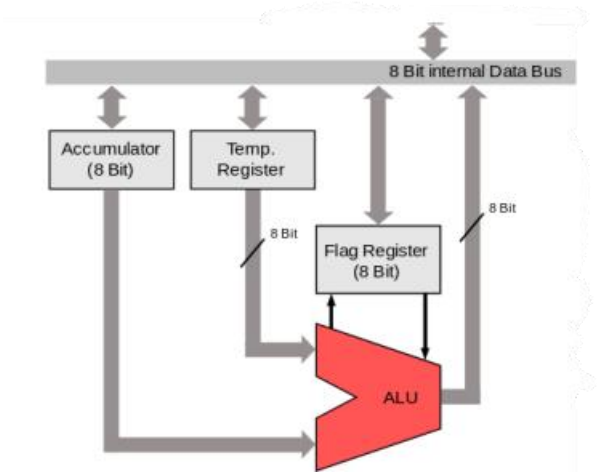
The 8085 microprocessor architecture provides the idea of the operations to be executed. It also tells about the working of the operations. The following are the main functional unit that constitutes the 8085 microprocessor architecture.



Arithmetic and Logic Unit (ALU)

The ALU, or the arithmetic and logic unit, performs various operations; Addition and Subtraction, Logical operations like AND, OR, or XOR, Complement (logical NOT), Increment, Decrement, Left shift, Right Shift, Clear, etc.

The ALU comprises the Accumulator, temporary registers, logic circuits, and flags. The result is always stored in an **Accumulator.**

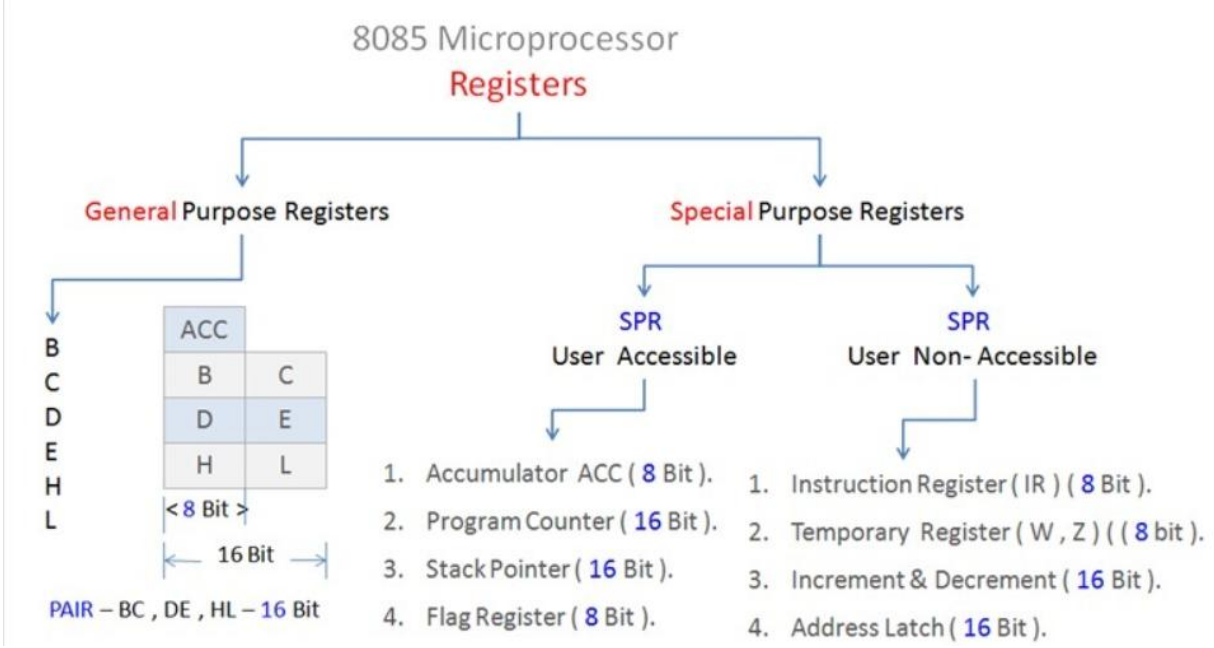


Accumulator

The Accumulator in the 8085 microprocessor is used to perform various operations. The operations can be arithmetic, logical, or Input/Output operations. The Accumulator is connected to the internal Data bus and the ALU. It is an 8-bit register and stores the result of the operations. It is denoted as register A.

Registers: The registers are a set of flip-flops, There are used to store the data, the 8085 microprocessor uses the following registers.

- **General Purpose Registers** : 8085 microprocessor consists of 6 general purpose registers. The registers are present inside the microprocessor. These registers stores 8-bit data to execute a program. The General purpose registers are denoted as B, C, D, E, H, and L. The registers are used as combined pairs as : BC, DE, and HL for performing 16-bit operations
- **Temporary registers:** These registers are used to store some temporary data. These registers are used in the ALU and are not accessible by the programmer.

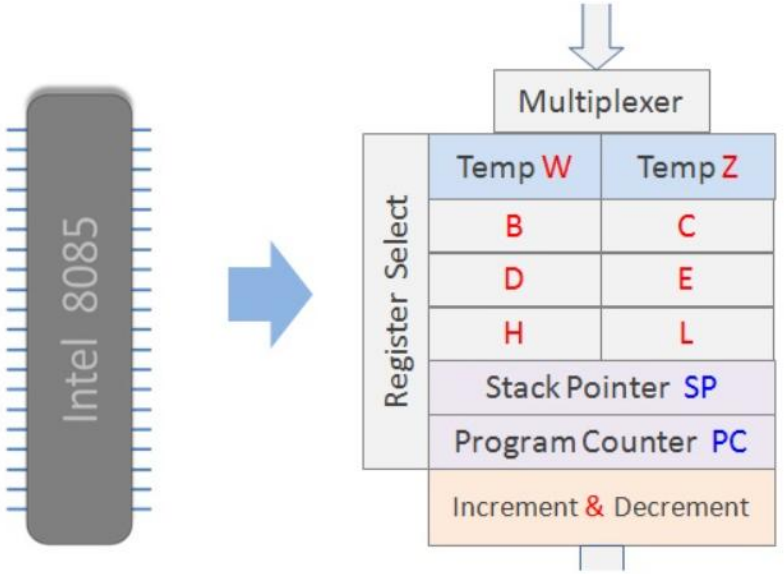


Program Counter (PC): The program counter is a 16-bit register to store addresses. The microprocessor uses it to sequence the instructions to be executed.

The function it performs is done using the opcode from one memory location. After that, increment the counter to the next instruction.

Stack Pointer (SP): The stack pointer is also a 16-bit register. The data in the stack pointer is stored sequentially. The stack pointer stores the address of the last element input of the stack.

With the addition of new data, the stack pointer is incremented. The stack pointer points to the removed memory location if an element is removed.



Instruction Register and Decoder

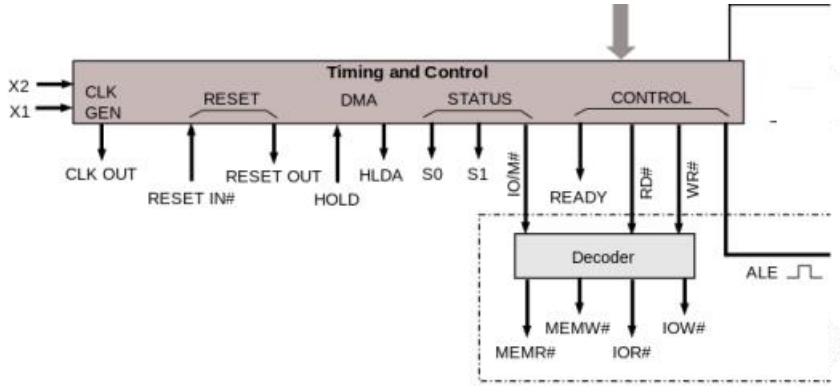
The instruction register and decoder are temporary storage devices. It stores the current instruction of a program. It is an 8-bit register. The instruction to be executed is sent here before execution. The decoder takes the instruction and interprets the instruction. The decoded instruction is then passed to the next stage.

- **Timing & Control Unit**

The Timing and Control units generate the signals. The generated signals are necessary for the execution of the instructions.

Controlling the data flow between the CPU and the other devices. It can also be used to control memory; It provides the timing signals, control, and status requires to operate memory and I/O devices

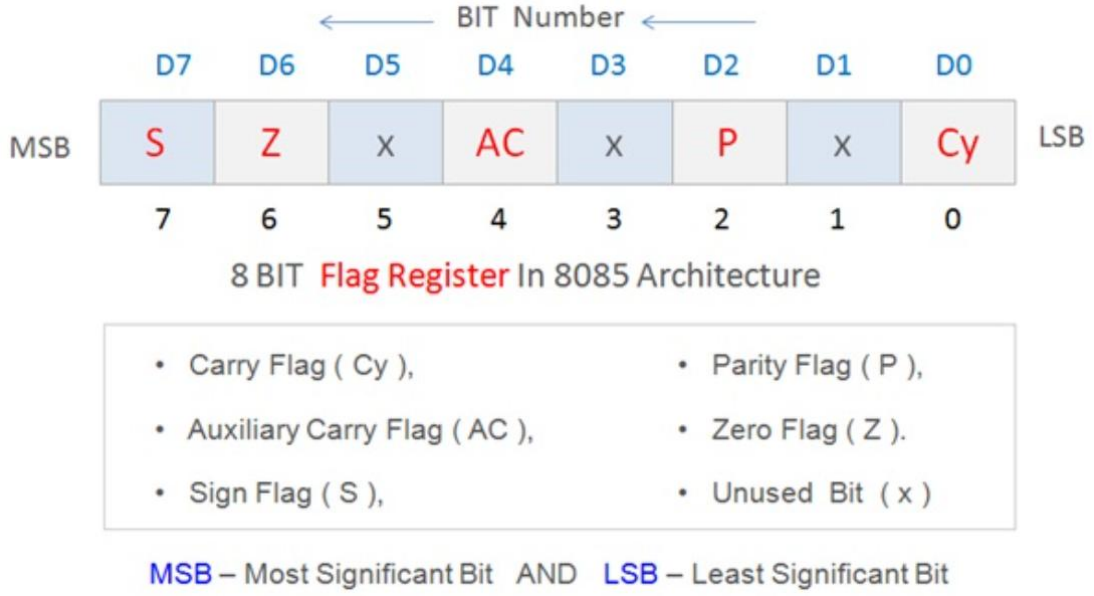
Some of the timing and control signals are the DMA signal, RESET signal, and STATUS signal



The Flag registers are used to define the status of the current result generated by the ALU. It does not hold the result. Thus, the **flags** are used to test the data conditions. The flag is an 8-bit register storing either 0 or 1.

- Sign (S) flag: Set if the result is negative
- Zero (Z) flag: Set if the result is zero.
- Auxiliary Carry (AC) flag: Set if there is a carry from bit 3 to bit 4, used in BCD operations.
- Parity (P) flag: Set if the result has an even number of 1s.
- Carry (CY) flag: Set if there is a carry out or borrow in arithmetic operations.

The unused bits are generally always 0.



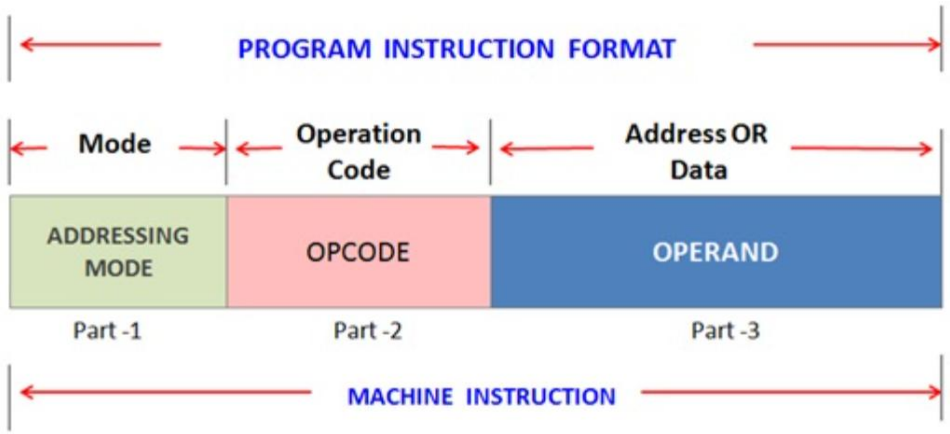
The flag register does not store data; it reflects the outcome of operations to guide decisions like jumps, loops, or arithmetic adjustments.

The instruction Cycle in 8085 Architecture:

Introduced by Intel in 1976, 8085 architecture is a 8 bit microprocessor, that has a set of instructions to be executed and these instructions for the execution has a set of series known as instruction cycle.

- Fetch: The CPU retrieves the memory-based instruction.
- Decode: To determine the operation, the fetched instruction is decoded.
- Execute: The CPU carries out the instruction's specified function.
- Store: Memory or registers are used to store results.

This cycle is repeated for every instruction, enabling the tasks of the program to be executed in order.



PART 1 – Addressing Mode - Rule For Operand - Data Or Address

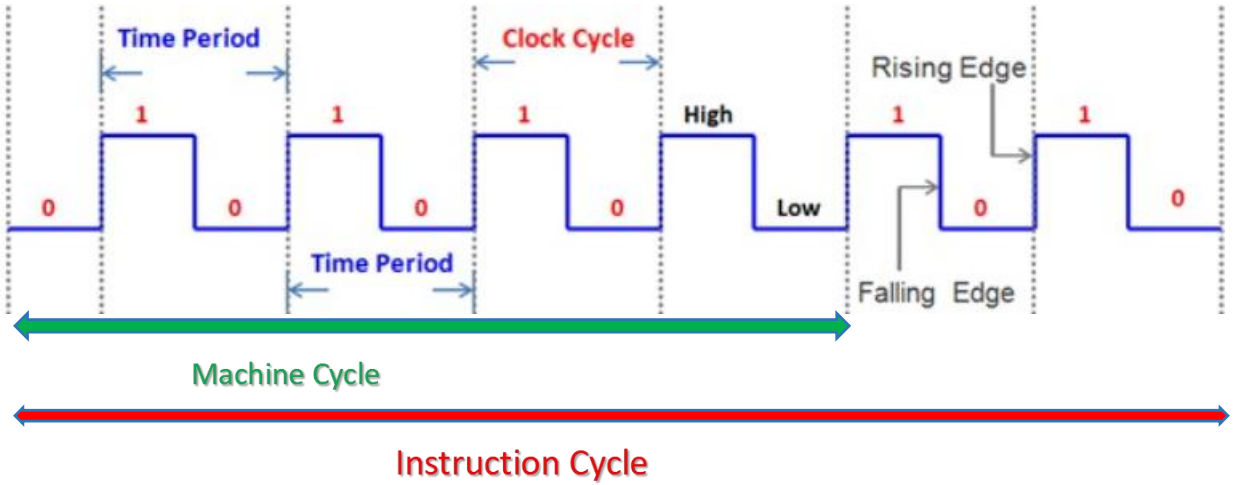
PART 2 – OPCODE - For Control Unit - Which Operation To Perform.

PART 3 – OPERAND - For ALU - On Data Operation To Be Performed.

T-State, Machine Cycle, and Instruction Cycle in Microprocessors

- **T-State:(Time period)** Basic clock period of the microprocessor.
- **Machine Cycle:** Time to perform a basic operation (read/write/fetch), made of several T-states.
- **Instruction Cycle:** Total time to execute an instruction, made of one or more machine cycles.

- Instruction Cycle=Sum of Machine Cycles for that instruction
- Machine Cycle=Sum of T-States required for that operation



A timing diagram shows the relationship between various control signals and the clock during the execution of an instruction in the 8085 microprocessor; It represents how the address bus, data bus, and control signals (like ALE, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, etc.) change with time while executing one instruction; Every instruction in the 8085 is divided into: Machine cycles, and each machine cycle is divided into T-states (T1, T2, T3, …).

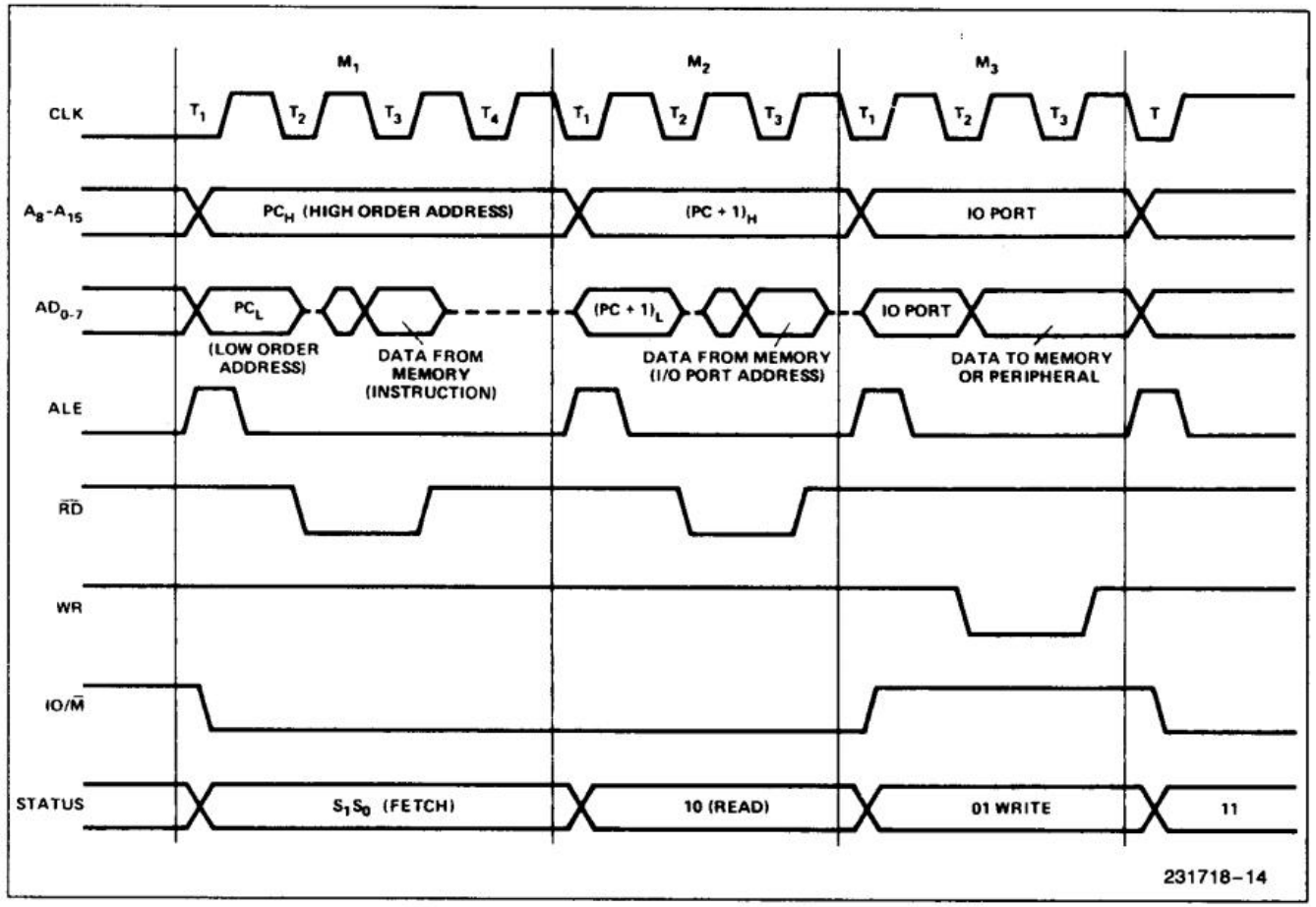


Figure . 8085AH Basic System Timing

Opcode Fetch Machine Cycle (8085)

- Every instruction in the 8085 has a 1-byte opcode stored in memory.
- The processor must fetch this opcode from memory before executing it.
- This process is called the Opcode Fetch Machine Cycle, and it is the first cycle of every instruction.

The cycle usually takes 4 T-states:

✓ The first 3 T-states are used to read the opcode from memory.

✓ The last T-state is used for internal processing (decoding the opcode).

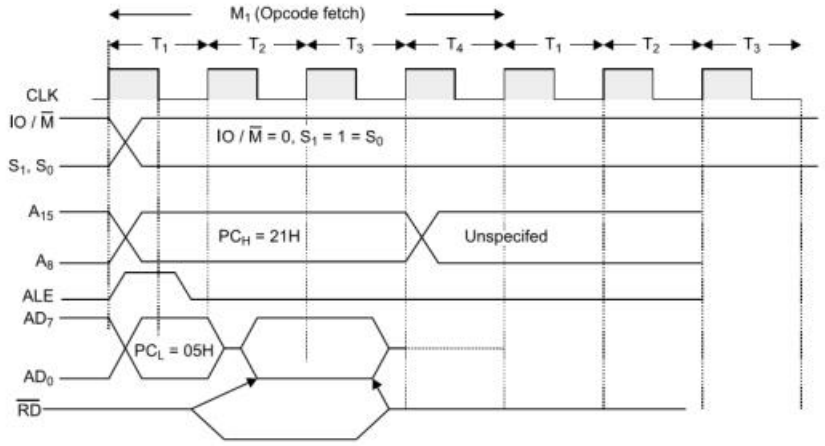


Fig. Opcode Fetch

Memory Read Machine Cycle of 8085

- A memory read machine cycle is executed by the processor to read a data byte from memory.
- The processor takes 3T states to perform this cycle.
- Instructions that have more than one byte word will use machine cycle after machine cycle to load the opcode.

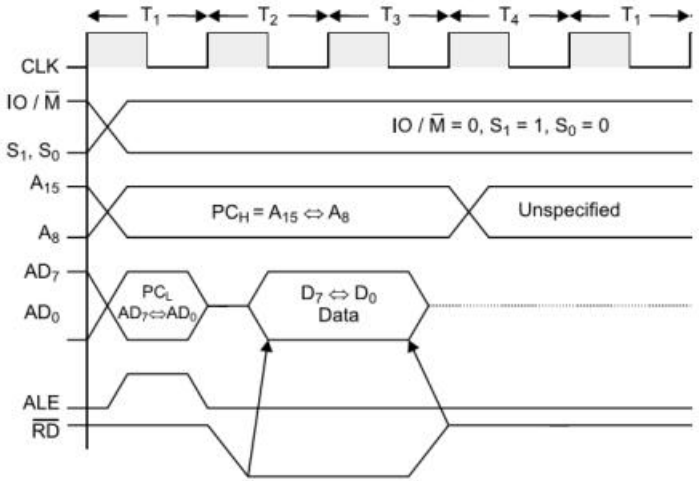


Fig. Memory Read Cycle

Memory Write Machine Cycle of 8085

- A write-to-memory machine cycle is executed by the processor to write a data byte to memory.
- The processor takes 3T states to perform this cycle.
- Instructions that have more than one byte word will use machine cycle after machine cycle to load the opcode.

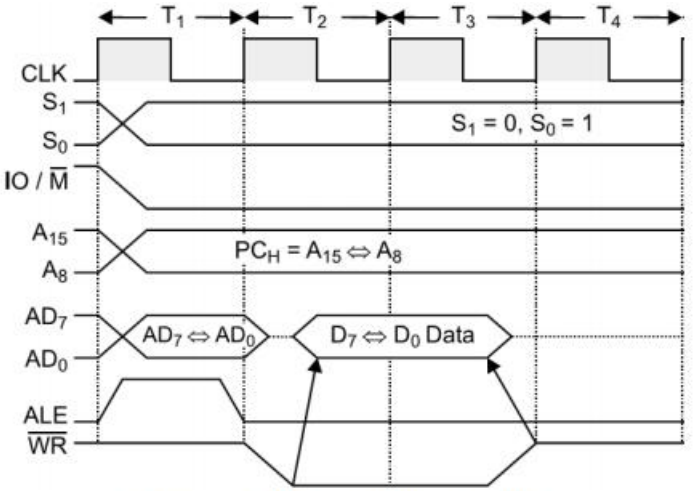


Fig. Memory Write Cycle

I/O Read Machine Cycle

- A reader I/O cycle is performed by the processor to read a data byte from an I/O port or peripheral that is I/O mapped in the system.
- The processor needs 3T states to execute this machine cycle.

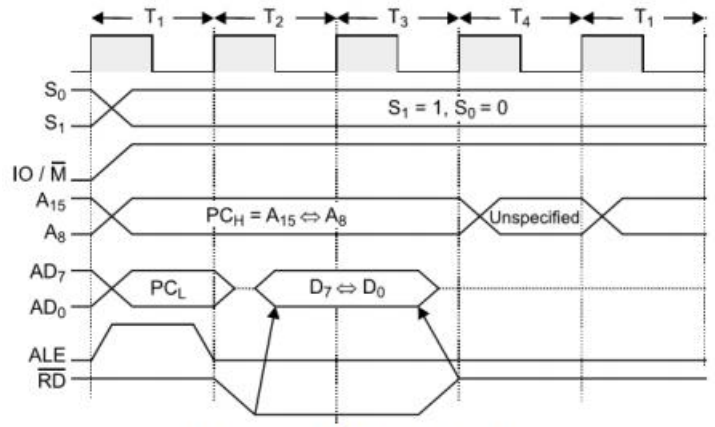


Fig. I/O Read Cycle

I/O Write Machine Cycle

- A writer's I/O cycle is executed by the processor to write a data byte to an I/O port or peripheral that is I/O mapped in the system.
- The processor needs 3T states to execute this machine cycle.

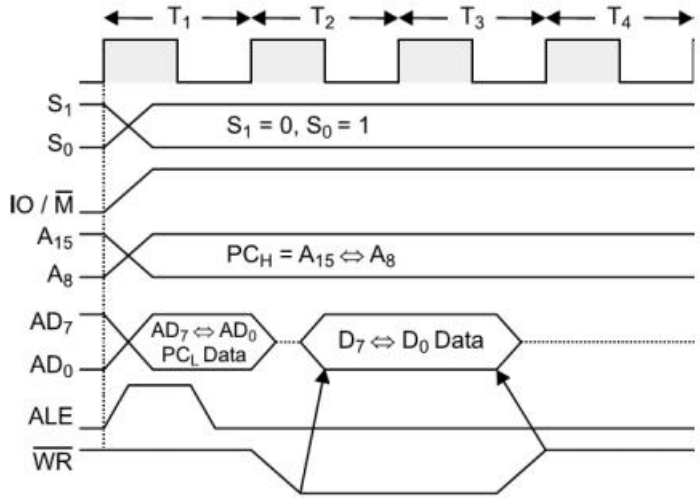


Fig. I/O Write Cycle